For Immediate Release

Press Release

For more information, please contact:

Eureka Technology
Simon Lau
President
(650)960-3800
simon@eurekatech.com

Cypress Semiconductor
Louie Yan
Public Relations Manager
(408)943-2817
LRY@cypress.com

Eureka Delivers PowerPC IP Cores to Cypress's IP Oasis™ Program

PowerPC Suite of Cores Targets Cypress's Delta39K™ CPLDs in Routers, Switches, Control-Plane Processors, Servers and Terminals

SAN JOSE, California…May 15, 2001 – Cypress Semiconductor (NYSE: CY) and Eureka Technology today announced the immediate availability of Eureka's suite of PowerPC intellectual property (IP) cores for the Cypress Delta39K™ family of complex programmable logic devices (CPLDs). Through the Cypress IP Oasis™ program, the PowerPC cores become part of a total CPLD solution for high-end communications systems, including routers, switches, control plane processors, servers, and terminals. The cores are optimized for use in Cypress's HDL-based *Warp*™ design tool, which integrates graphical capture, synthesis, fitting, simulation, and advanced design analysis capabilities.

"These IP cores from Eureka exemplify the growing support from third-party vendors for Cypress's Delta39K family and our commitment to provide our customers with a complete system solution," said Geoff Charubin, Cypress director of marketing. "As our CPLDs become more flexible with the introduction of additional IP support, their synergy with other Cypress devices increases. For example, designers can combine a Delta39K CPLD with a PowerPC core with our OC-48 PHY, No Bus Latency™ (NoBL™) and DualPort memories, and Zero Delay Buffers™ (ZDBs™) to build a LAN switch card solution."

"Eureka continues its drive to provide IP cores to Cypress's IP Oasis program, reinforcing our own strategy to support programmable devices with silicon-proven and production-proven IP," said Simon Lau, president of Eureka Technology. "We will continue our commitment to add to the growing library of CPU bus interface and system control function cores for the Delta39K devices, enabling designers to tackle design issues and speed their time-to-market."

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The IP Cores

- The PowerPC Bus Master – EP201 – is designed to initiate read/write data transfers on the PowerPC CPU host bus. It is typically connected to a DMA controller, bus snooping, or peripheral bus device such as PCI.
- The PowerPC Bus Slave – EP100 – is designed to be a target for CPU or other bus master access. It can be used as an interface between the CPU and the system's core logic, memory subsystem or peripheral device such as a PCI host bridge.
- The PowerPC Arbiter – EC300 – arbitrates between multiple bus masters on the PowerPC bus.

All Eureka PowerPC cores are compatible with the PowerPC, 603, 740, 750, and MPC8260 microprocessors.

Also available to designers using the Delta39K family of CPLDs are the Eureka PCI bus cores and SDRAM controller core.

IP Oasis

The IP Oasis program was designed to be the primary portal for data communications solutions built with IP cores and Cypress programmable logic devices, such as the Delta39K family of CPLDs and the PSI™ family of programmable PHYs. The IP cores are targeted at a variety of applications, including backplanes, line cards, switches, routers, 3G base stations, VoIP gateways, servers, mass storage equipment, interconnecting workstations, and video-transmission equipment. The cores are available as netlists optimized for use with Cypress's *Warp* development environment. IP Oasis, located at http://www.cypress.com/pld/ipoasis, allows users to view and select prequalified intellectual property cores and directs visitors to the IP vendor's sites for licenses and downloads.

Cypress Delta39K Family of CPLDs

Cypress's Delta39K CPLDs offer up to 350,000 usable gates, approximately ten times the size of today's largest CPLD. The family offers more embedded memory – 240 Kbits for the 100,000-gate Delta39K100 and 480 Kbits for the 200,000-gate Delta39K200 – than any other programmable logic device, including even the largest field-programmable gate arrays (FPGAs). Delta39K is also the first programmable logic device to embed First-In First-Out (FIFO) control and dual-port memory arbitration logic into each specialty memory block. This significantly reduces the logic required, increases the system performance, and speeds the design cycle of any application utilizing FIFO or dual-port memory.

Licensing and Availability

The Eureka IP cores for Delta39K CPLDs – for both the PowerPC and PCI buses – are available now for licensing directly through Eureka Technology's Web site, located at

http://ww.eurekatech.com/partners/cypress.htm. For more information on the Eureka cores portfolio, please call (650)960-3800 or visit the Eureka Technology Web site (http://www.eurekatech.com).

For more information on Cypress CPLDs, customers can call (800)858-1810 in the U.S. or (408)943-2600, or visit http://www.cypress.com/pld.

About Cypress

Cypress Semiconductor (NYSE: CY) is "Driving the Communications Revolution"™ by providing high-performance integrated circuit solutions to fast-growing markets, including data communications, telecommunications, computation, consumer products, and industrial control. With a focus on emerging communications applications, Cypress's product portfolios include networking-optimized and micropower static RAMs; high-bandwidth multi-port and FIFO memories; high-density programmable logic devices; timing technology for PCs and other digital systems; and controllers for Universal Serial Bus (USB). More information about Cypress is accessible electronically on the company's worldwide Web site at http://www.cypress.com or by CD-ROM (call 1-800-858-1810).

"Safe Harbor" Statement under the Private Securities Litigation Reform Act of 1995: Statements herein that are not historical facts are "forward-looking statements" involving risks and uncertainties, including by not limited to: the effect of global economic conditions, shifts in supply and demand, market acceptance, the impact of competitive products and pricing, product development, commercialization and technological difficulties, and capacity and supply constraints. Please refer to Cypress's Securities and Exchange Commission filings for a discussion of such risks.

About Eureka Technology

Eureka Technology is a leading intellectual property (IP) provider for PLD and ASIC designers. The company offers a wide range of silicon-proved system core logic functions and peripheral functions for systems based on PCI bus, PowerPC, ARM, MIPS, ARC, or SH2-4 CPUs. These IP cores are designed to improve the design time-to-market delay, eliminate design risks, and reduce development costs. Founded in 1993, the company has a strong customer base in the United States, Japan and Europe. For more information about the company, please visit the Web site at http://www.eurekatech.com or send email to info@eurekatech.com.

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